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Term	Documents
(8 AND 16).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	4
(L16 AND L8).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	4

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L17

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<u>Set Name</u> side by side	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u> result set
<i>DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L17</u>	L16 and l8	4	<u>L17</u>
<u>L16</u>	l10 or l11 or l12 or l13 or l14 or L15	2315	<u>L16</u>
<u>L15</u>	(711/219)!	482	<u>L15</u>
<u>L14</u>	(711/216)!	317	<u>L14</u>
<u>L13</u>	(711/211)!	436	<u>L13</u>
<u>L12</u>	(711/213)!	571	<u>L12</u>
<u>L11</u>	(711/209)!	609	<u>L11</u>
<u>L10</u>	(711/204)!	348	<u>L10</u>
<u>L9</u>	L8	33	<u>L9</u>
<i>DB=USPT; PLUR=YES; OP=OR</i>			
<u>L8</u>	L3 and branch\$3	33	<u>L8</u>
<u>L7</u>	L1 and branch\$3	63	<u>L7</u>
<u>L6</u>	L5 and branch\$3	2	<u>L6</u>
<u>L5</u>	L1 and index near9 (compar\$6)	6	<u>L5</u>
<u>L4</u>	L1 near9 (compar\$6) and index	2	<u>L4</u>
<u>L3</u>	L1 and index	54	<u>L3</u>
<u>L2</u>	L1 near15 index	1	<u>L2</u>
<u>L1</u>	(conflict\$3 or contend\$3) near6 bank\$1 near5 memory	164	<u>L1</u>

END OF SEARCH HISTORY

WEST[Generate Collection](#)[Print](#)

Search Results - Record(s) 1 through 3 of 3 returned.

☐ 1. Document ID: US 6564315 B1

L10: Entry 1 of 3

File: USPT

May 13, 2003

US-PAT-NO: 6564315

DOCUMENT-IDENTIFIER: US 6564315 B1

TITLE: Scheduler which discovers non-speculative nature of an instruction after issuing and reissues the instruction

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 2. Document ID: US 6195744 B1

L10: Entry 2 of 3

File: USPT

Feb 27, 2001

US-PAT-NO: 6195744

DOCUMENT-IDENTIFIER: US 6195744 B1

**** See image for Certificate of Correction ****

TITLE: Unified multi-function operation scheduler for out-of-order execution in a superscaler processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 3. Document ID: US 5884059 A

L10: Entry 3 of 3

File: USPT

Mar 16, 1999

US-PAT-NO: 5884059

DOCUMENT-IDENTIFIER: US 5884059 A

TITLE: Unified multi-function operation scheduler for out-of-order execution in a superscalar processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

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Term	Documents
(1 AND 9).USPT.	3
(L1 AND L9).USPT.	3

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WEST[Help](#)[Logout](#)[Interrupt](#)[Main Menu](#)[Search Form](#)[Posting Counts](#)[Show S Numbers](#)[Edit S Numbers](#)[Preferences](#)[Cases](#)**Search Results -**

Term	Documents
10.USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	3
(L10).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	3

Database:

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Search:

L11

[Refine Search](#)[Recall Text](#)[Clear](#)**Search History****DATE:** Thursday, November 13, 2003 [Printable Copy](#) [Create Case](#)

<u>Set Name</u>	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u>
side by side			result set
	<i>DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>		
<u>L11</u>	L10	3	<u>L11</u>
	<i>DB=USPT; PLUR=YES; OP=OR</i>		
<u>L10</u>	l1 and L9	3	<u>L10</u>
<u>L9</u>	l5 or l6 or l7 or l8L8	495	<u>L9</u>
<u>L8</u>	((712/236)!.CCLS.)	101	<u>L8</u>
<u>L7</u>	((712/235)!.CCLS.)	101	<u>L7</u>
<u>L6</u>	((712/240)!.CCLS.)	198	<u>L6</u>
<u>L5</u>	((712/239)!.CCLS.)	293	<u>L5</u>
<u>L4</u>	L2 and 3 near8 4	38	<u>L4</u>
<u>L3</u>	L2 and 3 and 4	54	<u>L3</u>
<u>L2</u>	L1 and index	54	<u>L2</u>
<u>L1</u>	(conflict\$3 or contend\$3) near6 bank\$1 near5 memory	164	<u>L1</u>

END OF SEARCH HISTORY

WEST[Generate Collection](#)[Print](#)**Search Results - Record(s) 1 through 20 of 28 returned.**☐ 1. Document ID: US 20030208723 A1

L2: Entry 1 of 28

File: PGPB

Nov 6, 2003

PGPUB-DOCUMENT-NUMBER: 20030208723

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030208723 A1

TITLE: Automated processor generation system for designing a configurable processor and method for the same

PUBLICATION-DATE: November 6, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Killian, Earl A.	Los Altos Hills	CA	US	
Gonzalez, Ricardo E.	Menlo Park	CA	US	
Dixit, Ashish B.	Mountain View	CA	US	
Lam, Monica	Menlo Park	CA	US	
Lichtenstein, Walter D.	Belmont	MA	US	
Rowen, Christopher	Santa Cruz	CA	US	
Ruttenberg, John C.	Newton	MA	US	
Wilson, Robert P.	Palo Alto	CA	US	
Wang, Albert Ren-Rui	Fremont	CA	US	
Maydan, Dror Eliezer	Palo Alto	CA	US	

US-CL-CURRENT: 716/1

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWOC
Draw Desc	Image										

☐ 2. Document ID: US 20020194464 A1

L2: Entry 2 of 28

File: PGPB

Dec 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020194464

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020194464 A1

TITLE: Speculative branch target address cache with selective override by secondary predictor based on branch instruction type

PUBLICATION-DATE: December 19, 2002

INVENTOR-INFORMATION:

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	W00C
Draw Desc	Image										

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	K00C
Draw Desc	Image										

[illegible]

☐ 5. Document ID: US 20020194461 A1

L2: Entry 5 of 28

File: PGPB

Dec 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020194461

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020194461 A1

TITLE: Speculative branch target address cache

PUBLICATION-DATE: December 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Henry, G. Glenn	Austin	TX	US	
McDonald, Thomas C.	Austin	TX	US	

US-CL-CURRENT: 712/238

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw	Desc	Image								

☐ 6. Document ID: US 20020194460 A1

L2: Entry 6 of 28

File: PGPB

Dec 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020194460

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020194460 A1

TITLE: Apparatus, system and method for detecting and correcting erroneous speculative branch target address cache branches

PUBLICATION-DATE: December 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Henry, G. Glenn	Austin	TX	US	
McDonald, Thomas C.	Austin	TX	US	
Parks, Terry	Austin	TX	US	

US-CL-CURRENT: 712/238

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw	Desc	Image								

☐ 7. Document ID: US 20020188834 A1

L2: Entry 7 of 28

File: PGPB

Dec 12, 2002

PGPUB-DOCUMENT-NUMBER: 20020188834

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020188834 A1

TITLE: Apparatus and method for target address replacement in speculative branch target address cache

PUBLICATION-DATE: December 12, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
McDonald, Thomas C.	Austin	TX	US	
Parks, Terry	Austin	TX	US	

US-CL-CURRENT: 712/238

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 8. Document ID: US 20020188833 A1

L2: Entry 8 of 28

File: PGPB

Dec 12, 2002

PGPUB-DOCUMENT-NUMBER: 20020188833

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020188833 A1

TITLE: Dual call/return stack branch prediction system

PUBLICATION-DATE: December 12, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Henry, G. Glenn	Austin	TX	US	
McDonald, Thomas C.	Austin	TX	US	

US-CL-CURRENT: 712/236; 712/242

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 9. Document ID: US 20020144176 A1

L2: Entry 9 of 28

File: PGPB

Oct 3, 2002

PGPUB-DOCUMENT-NUMBER: 20020144176

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020144176 A1

TITLE: Method and apparatus for improving reliability in microprocessors

PUBLICATION-DATE: October 3, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Smith, Ronald D.	Phoenix	AZ	US	

US-CL-CURRENT: 714/11

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 10. Document ID: US 6550004 B1

L2: Entry 10 of 28

File: USPT

Apr 15, 2003

US-PAT-NO: 6550004

DOCUMENT-IDENTIFIER: US 6550004 B1

TITLE: Hybrid branch predictor with improved selector table update mechanism

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 11. Document ID: US 6526502 B1

L2: Entry 11 of 28

File: USPT

Feb 25, 2003

US-PAT-NO: 6526502

DOCUMENT-IDENTIFIER: US 6526502 B1

TITLE: Apparatus and method for speculatively updating global branch history with branch prediction prior to resolution of branch outcome

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 12. Document ID: US 6477683 B1

L2: Entry 12 of 28

File: USPT

Nov 5, 2002

US-PAT-NO: 6477683

DOCUMENT-IDENTIFIER: US 6477683 B1

TITLE: Automated processor generation system for designing a configurable processor and method for the same

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 13. Document ID: US 6421774 B1

L2: Entry 13 of 28

File: USPT

Jul 16, 2002

US-PAT-NO: 6421774

DOCUMENT-IDENTIFIER: US 6421774 B1

TITLE: Static branch predictor using opcode of instruction preceding conditional branch

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 14. Document ID: US 6347369 B1

L2: Entry 14 of 28

File: USPT

Feb 12, 2002

US-PAT-NO: 6347369

DOCUMENT-IDENTIFIER: US 6347369 B1

TITLE: Method and circuit for single cycle multiple branch history table access

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 15. Document ID: US 6272624 B1

L2: Entry 15 of 28

File: USPT

Aug 7, 2001

US-PAT-NO: 6272624

DOCUMENT-IDENTIFIER: US 6272624 B1

TITLE: Method and apparatus for predicting multiple conditional branches

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 16. Document ID: US 6247122 B1

L2: Entry 16 of 28

File: USPT

Jun 12, 2001

US-PAT-NO: 6247122

DOCUMENT-IDENTIFIER: US 6247122 B1

TITLE: Method and apparatus for performing branch prediction combining static and dynamic branch predictors

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMIC

☐ 17. Document ID: US 6189091 B1

L2: Entry 17 of 28

File: USPT

Feb 13, 2001

US-PAT-NO: 6189091

DOCUMENT-IDENTIFIER: US 6189091 B1

TITLE: Apparatus and method for speculatively updating global history and restoring same on branch misprediction detection

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 18. Document ID: US 6138223 A

L2: Entry 18 of 28

File: USPT

Oct 24, 2000

US-PAT-NO: 6138223

DOCUMENT-IDENTIFIER: US 6138223 A

**** See image for Certificate of Correction ****

TITLE: Absolute address history table index generation for predicting instruction and operand cache accesses

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 19. Document ID: US 6138215 A

L2: Entry 19 of 28

File: USPT

Oct 24, 2000

US-PAT-NO: 6138215

DOCUMENT-IDENTIFIER: US 6138215 A

TITLE: Method for absolute address history table synonym resolution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

☐ 20. Document ID: US 5938761 A

L2: Entry 20 of 28

File: USPT

Aug 17, 1999

US-PAT-NO: 5938761

DOCUMENT-IDENTIFIER: US 5938761 A

TITLE: Method and apparatus for branch target prediction

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								

KMC

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Term	Documents
TABLE	1277538
TABLES	251187
INDEX\$3	0
INDEX	1152902
INDEXA	11
INDEXAL	1
INDEXAND	4
INDEXAPP	1
INDEXARG	1
INDEXART	3
INDEXAS	1
(TABLE NEAR8 INDEX\$3 NEAR15 (BANK\$1 OR ARRAY\$1) AND L1).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	28

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WEST[Generate Collection](#)[Print](#)**Search Results - Record(s) 21 through 28 of 28 returned.**☐ 21. Document ID: US 5696958 A

L2: Entry 21 of 28

File: USPT

Dec 9, 1997

US-PAT-NO: 5696958

DOCUMENT-IDENTIFIER: US 5696958 A

**** See image for Certificate of Correction ****

TITLE: Method and apparatus for reducing delays following the execution of a branch instruction in an instruction pipeline

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw Desc	Image									

☐ 22. Document ID: US 5652889 A

L2: Entry 22 of 28

File: USPT

Jul 29, 1997

US-PAT-NO: 5652889

DOCUMENT-IDENTIFIER: US 5652889 A

TITLE: Alternate execution and interpretation of computer program having code at unknown locations due to transfer instructions having computed destination addresses

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw Desc	Image									

☐ 23. Document ID: US 5649203 A

L2: Entry 23 of 28

File: USPT

Jul 15, 1997

US-PAT-NO: 5649203

DOCUMENT-IDENTIFIER: US 5649203 A

TITLE: Translating, executing, and re-translating a computer program for finding and translating program code at unknown program addresses

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw Desc	Image									

☐ 24. Document ID: US 5613132 A

L2: Entry 24 of 28

File: USPT

Mar 18, 1997

US-PAT-NO: 5613132

DOCUMENT-IDENTIFIER: US 5613132 A

**** See image for Certificate of Correction ****

TITLE: Integer and floating point register alias table within processor device

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KM/C
Draw Desc	Image									

☐ 25. Document ID: US 5507030 A

L2: Entry 25 of 28

File: USPT

Apr 9, 1996

US-PAT-NO: 5507030

DOCUMENT-IDENTIFIER: US 5507030 A

TITLE: Successive translation, execution and interpretation of computer program having code at unknown locations due to execution transfer instructions having computed destination addresses

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KM/C
Draw Desc	Image									

☐ 26. Document ID: US 5428786 A

L2: Entry 26 of 28

File: USPT

Jun 27, 1995

US-PAT-NO: 5428786

DOCUMENT-IDENTIFIER: US 5428786 A

TITLE: Branch resolution via backward symbolic execution

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KM/C
Draw Desc	Image									

☐ 27. Document ID: US 5317740 A

L2: Entry 27 of 28

File: USPT

May 31, 1994

US-PAT-NO: 5317740

DOCUMENT-IDENTIFIER: US 5317740 A

TITLE: Alternate and iterative analysis of computer programs for locating translatable code by resolving callbacks and other conflicting mutual dependencies

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KM/C
Draw Desc	Image									

☐ 28. Document ID: US 5287490 A

L2: Entry 28 of 28

File: USPT

Feb 15, 1994

US-PAT-NO: 5287490

DOCUMENT-IDENTIFIER: US 5287490 A

TITLE: Identifying plausible variable length machine code of selecting address in numerical sequence, decoding code strings, and following execution transfer paths

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw	Desc	Image								

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Term	Documents
TABLE	1277538
TABLES	251187
INDEX\$3	0
INDEX	1152902
INDEXA	11
INDEXAL	1
INDEXAND	4
INDEXAPP	1
INDEXARG	1
INDEXART	3
INDEXAS	1
(TABLE NEAR8 INDEX\$3 NEAR15 (BANK\$1 OR ARRAY\$1) AND L1).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	28

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Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
Draw Desc	Image								
KWIC									

☐ 3. Document ID: US 20020188833 A1

L15: Entry 3 of 11

File: PGPB

Dec 12, 2002

PGPUB-DOCUMENT-NUMBER: 20020188833
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020188833 A1

TITLE: Dual call/return stack branch prediction system

PUBLICATION-DATE: December 12, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Henry, G. Glenn	Austin	TX	US	
McDonald, Thomas C.	Austin	TX	US	

US-CL-CURRENT: 712/236; 712/242

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 4. Document ID: US 6550004 B1

L15: Entry 4 of 11

File: USPT

Apr 15, 2003

US-PAT-NO: 6550004
DOCUMENT-IDENTIFIER: US 6550004 B1

TITLE: Hybrid branch predictor with improved selector table update mechanism

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 5. Document ID: US 6526502 B1

L15: Entry 5 of 11

File: USPT

Feb 25, 2003

US-PAT-NO: 6526502
DOCUMENT-IDENTIFIER: US 6526502 B1

TITLE: Apparatus and method for speculatively updating global branch history with branch prediction prior to resolution of branch outcome

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

☐ 6. Document ID: US 6421774 B1

L15: Entry 6 of 11

File: USPT

Jul 16, 2002

US-PAT-NO: 6421774
DOCUMENT-IDENTIFIER: US 6421774 B1

TITLE: Static branch predictor using opcode of instruction preceding conditional branch

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMIC
Draw Desc	Image									

☐ 7. Document ID: US 6347369 B1

L15: Entry 7 of 11

File: USPT

Feb 12, 2002

US-PAT-NO: 6347369

DOCUMENT-IDENTIFIER: US 6347369 B1

TITLE: Method and circuit for single cycle multiple branch history table access

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMIC
Draw Desc	Image									

☐ 8. Document ID: US 6272624 B1

L15: Entry 8 of 11

File: USPT

Aug 7, 2001

US-PAT-NO: 6272624

DOCUMENT-IDENTIFIER: US 6272624 B1

TITLE: Method and apparatus for predicting multiple conditional branches

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMIC
Draw Desc	Image									

☐ 9. Document ID: US 6247122 B1

L15: Entry 9 of 11

File: USPT

Jun 12, 2001

US-PAT-NO: 6247122

DOCUMENT-IDENTIFIER: US 6247122 B1

TITLE: Method and apparatus for performing branch prediction combining static and dynamic branch predictors

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMIC
Draw Desc	Image									

☐ 10. Document ID: US 6189091 B1

L15: Entry 10 of 11

File: USPT

Feb 13, 2001

US-PAT-NO: 6189091

DOCUMENT-IDENTIFIER: US 6189091 B1

TITLE: Apparatus and method for speculatively updating global history and restoring

same on branch misprediction detection

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw Desc	Image									

☐ 11. Document ID: US 5696958 A

L15: Entry 11 of 11

File: USPT

Dec 9, 1997

US-PAT-NO: 5696958

DOCUMENT-IDENTIFIER: US 5696958 A

**** See image for Certificate of Correction ****

TITLE: Method and apparatus for reducing delays following the execution of a branch instruction in an instruction pipeline

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
Draw Desc	Image									

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Term	Documents
(2 AND 14).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	11
(L14 AND L2).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	11

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Term	Documents
BRANCH	122993
BRANCHES	80517
PREDICT\$3	0
PREDICT	39983
PREDICTA	8
PREDICTABE	1
PREDICTAND	1
PREDICTATE	4
PREDICTBLE	1
PREDICTD	2
PREDICTE	9
(L1 NEAR8 BRANCH NEAR4 PREDICT\$3).USPT.	21

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Search:

L3

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<u>Set Name</u>	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u>
side by side			result set
<i>DB=USPT; PLUR=YES; OP=OR</i>			
<u>L3</u>	L1 near8 branch near4 predict\$3	21	<u>L3</u>
<u>L2</u>	L1 and branch near4 predict\$3	409	<u>L2</u>
<u>L1</u>	(one or single) near3 port\$2	79352	<u>L1</u>

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Term	Documents
BRANCH\$3	0
BRANCH	122993
BRANCHA	1
BRANCHAD	1
BRANCHADD	1
BRANCHAND	2
BRANCHAR	1
BRANCHARD	4
BRANCHARI	1
BRANCHAT	1
BRANCHAUD	14
(L12 AND BRANCH\$3).USPT.	35

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EPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search:

L13

[Refine Search](#)[Recall Text](#)[Clear](#)**Search History**

DATE: Wednesday, November 12, 2003 [Printable Copy](#) [Create Case](#)

Set Name Query
side by side

Hit Count Set Name
result set

DB=USPT; PLUR=YES; OP=OR

<u>L13</u>	L12 and branch\$3	35	<u>L13</u>
<u>L12</u>	L1 near4 bank\$1 near2 memory	107	<u>L12</u>
<u>L11</u>	L1 near4 bank\$1 near3 memory	113	<u>L11</u>
<u>L10</u>	L1 near4 bank\$1	301	<u>L10</u>
<u>L9</u>	L8 not 14	23	<u>L9</u>
<u>L8</u>	L1 near6 bank\$1 and branch near5 prediction	23	<u>L8</u>
<u>L7</u>	L1 near6 bank\$1	343	<u>L7</u>
<u>L6</u>	L5 not 14	1	<u>L6</u>
<u>L5</u>	L1 near12 branch near7 predict\$3	22	<u>L5</u>
<u>L4</u>	L1 near8 branch near6 predict\$3	21	<u>L4</u>
<u>L3</u>	L1 near8 branch near4 predict\$3	21	<u>L3</u>
<u>L2</u>	L1 and branch near4 predict\$3	409	<u>L2</u>
<u>L1</u>	(one or single) near3 port\$2	79352	<u>L1</u>

END OF SEARCH HISTORY

WEST[Generate Collection](#)[Print](#)**Search Results - Record(s) 1 through 4 of 4 returned.**☐ 1. Document ID: US 6591345 B1

L17: Entry 1 of 4

File: USPT

Jul 8, 2003

US-PAT-NO: 6591345

DOCUMENT-IDENTIFIER: US 6591345 B1

TITLE: Method for ensuring maximum bandwidth on accesses to strided vectors in a bank-interleaved cache

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

☐ 2. Document ID: US 6574724 B1

L17: Entry 2 of 4

File: USPT

Jun 3, 2003

US-PAT-NO: 6574724

DOCUMENT-IDENTIFIER: US 6574724 B1

TITLE: Microprocessor with non-aligned scaled and unscaled addressing

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

☐ 3. Document ID: US 6546453 B1

L17: Entry 3 of 4

File: USPT

Apr 8, 2003

US-PAT-NO: 6546453

DOCUMENT-IDENTIFIER: US 6546453 B1

TITLE: Proprogrammable DRAM address mapping mechanism

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

☐ 4. Document ID: US 6539467 B1

L17: Entry 4 of 4

File: USPT

Mar 25, 2003

US-PAT-NO: 6539467

DOCUMENT-IDENTIFIER: US 6539467 B1

TITLE: Microprocessor with non-aligned memory access

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC
Draw Desc	Image										

Generate Collection

Print

Term	Documents
(8 AND 16).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	4
(L16 AND L8).USPT,PGPB,JPAB,EPAB,DWPI,TDBD.	4

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Search Results - Record(s) 1 through 20 of 21 returned.

☐ 1. Document ID: US 6604190 B1

Using default format because multiple data bases are involved.

L8: Entry 1 of 21

File: USPT

Aug 5, 2003

US-PAT-NO: 6604190

DOCUMENT-IDENTIFIER: US 6604190 B1

TITLE: Data address prediction structure and a method for operating the same

DATE-ISSUED: August 5, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tran; Thang M.	Austin	TX		

US-CL-CURRENT: 712/207; 712/204, 712/240

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw. De
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☐ 2. Document ID: US 6230261 B1

L8: Entry 2 of 21

File: USPT

May 8, 2001

US-PAT-NO: 6230261

DOCUMENT-IDENTIFIER: US 6230261 B1

TITLE: Method and apparatus for predicting conditional branch instruction outcome based on branch condition test type

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw. De
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☐ 3. Document ID: US 6189068 B1

L8: Entry 3 of 21

File: USPT

Feb 13, 2001

US-PAT-NO: 6189068

DOCUMENT-IDENTIFIER: US 6189068 B1

TITLE: Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle

h e b b g e e e f e ef b e

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 4. Document ID: US 6079006 A

L8: Entry 4 of 21

File: USPT

Jun 20, 2000

US-PAT-NO: 6079006

DOCUMENT-IDENTIFIER: US 6079006 A

TITLE: Stride-based data address prediction structure

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 5. Document ID: US 6073230 A

L8: Entry 5 of 21

File: USPT

Jun 6, 2000

US-PAT-NO: 6073230

DOCUMENT-IDENTIFIER: US 6073230 A

TITLE: Instruction fetch unit configured to provide sequential way prediction for sequential instruction fetches

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 6. Document ID: US 5987561 A

L8: Entry 6 of 21

File: USPT

Nov 16, 1999

US-PAT-NO: 5987561

DOCUMENT-IDENTIFIER: US 5987561 A

TITLE: Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 7. Document ID: US 5978907 A

L8: Entry 7 of 21

File: USPT

Nov 2, 1999

US-PAT-NO: 5978907

DOCUMENT-IDENTIFIER: US 5978907 A

TITLE: Delayed update register for an array

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 8. Document ID: US 5968169 A

L8: Entry 8. of 21

File: USPT

Oct 19, 1999

US-PAT-NO: 5968169

DOCUMENT-IDENTIFIER: US 5968169 A

TITLE: Superscalar microprocessor stack structure for judging validity of predicted subroutine return addresses

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 9. Document ID: US 5881278 A

L8: Entry 9 of 21

File: USPT

Mar 9, 1999

US-PAT-NO: 5881278

DOCUMENT-IDENTIFIER: US 5881278 A

**** See image for Certificate of Correction ****

TITLE: Return address prediction system which adjusts the contents of return stack storage to enable continued prediction after a mispredicted branch

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 10. Document ID: US 5878255 A

L8: Entry 10 of 21

File: USPT

Mar 2, 1999

US-PAT-NO: 5878255

DOCUMENT-IDENTIFIER: US 5878255 A

TITLE: Update unit for providing a delayed update to a branch prediction array

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 11. Document ID: US 5875324 A

L8: Entry 11 of 21

File: USPT

Feb 23, 1999

US-PAT-NO: 5875324

DOCUMENT-IDENTIFIER: US 5875324 A

TITLE: Superscalar microprocessor which delays update of branch prediction information in response to branch misprediction until a subsequent idle clock

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 12. Document ID: US 5860104 A

L8: Entry 12 of 21

File: USPT

Jan 12, 1999

US-PAT-NO: 5860104

DOCUMENT-IDENTIFIER: US 5860104 A

TITLE: Data cache which speculatively updates a predicted data cache storage location with store data and subsequently corrects mispredicted updates

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 13. Document ID: US 5857104 A

L8: Entry 13 of 21

File: USPT

Jan 5, 1999

US-PAT-NO: 5857104

DOCUMENT-IDENTIFIER: US 5857104 A

TITLE: Synthetic dynamic branch prediction

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 14. Document ID: US 5854921 A

L8: Entry 14 of 21

File: USPT

Dec 29, 1998

US-PAT-NO: 5854921

DOCUMENT-IDENTIFIER: US 5854921 A

TITLE: Stride-based data address prediction structure

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 15. Document ID: US 5822574 A

L8: Entry 15 of 21

File: USPT

Oct 13, 1998

US-PAT-NO: 5822574

DOCUMENT-IDENTIFIER: US 5822574 A

TITLE: Functional unit with a pointer for mispredicted resolution, and a superscalar microprocessor employing the same

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 16. Document ID: US 5794028 A

L8: Entry 16 of 21

File: USPT

Aug 11, 1998

US-PAT-NO: 5794028
DOCUMENT-IDENTIFIER: US 5794028 A

TITLE: Shared branch prediction structure

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 17. Document ID: US 5764946 A

L8: Entry 17 of 21

File: USPT

Jun 9, 1998

US-PAT-NO: 5764946
DOCUMENT-IDENTIFIER: US 5764946 A

TITLE: Superscalar microprocessor employing a way prediction unit to predict the way of an instruction fetch address and to concurrently provide a branch prediction address corresponding to the fetch address

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 18. Document ID: US 5752069 A

L8: Entry 18 of 21

File: USPT

May 12, 1998

US-PAT-NO: 5752069
DOCUMENT-IDENTIFIER: US 5752069 A

**** See image for Certificate of Correction ****

TITLE: Superscalar microprocessor employing away prediction structure

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 19. Document ID: US 5655122 A

L8: Entry 19 of 21

File: USPT

Aug 5, 1997

US-PAT-NO: 5655122
DOCUMENT-IDENTIFIER: US 5655122 A

TITLE: Optimizing compiler with static prediction of branch probability, branch frequency and function frequency

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 20. Document ID: US 5414822 A

L8: Entry 20 of 21

File: USPT

May 9, 1995

US-PAT-NO: 5414822
DOCUMENT-IDENTIFIER: US 5414822 A

TITLE: Method and apparatus for branch prediction using branch prediction table
with improved branch prediction effectiveness

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMIC	Draw De
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Term	Documents
(1 AND 6).PGPB,USPT.	21
(L1 AND L6).PGPB,USPT.	21

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Search Results - Record(s) 1 through 14 of 14 returned.

☐ 1. Document ID: US 6604190 B1

Using default format because multiple data bases are involved.

L12: Entry 1 of 14

File: USPT

Aug 5, 2003

US-PAT-NO: 6604190

DOCUMENT-IDENTIFIER: US 6604190 B1

TITLE: Data address prediction structure and a method for operating the same

DATE-ISSUED: August 5, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tran; Thang M.	Austin	TX		

US-CL-CURRENT: 712/207; 712/204, 712/240

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Drawings
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☐ 2. Document ID: US 6189068 B1

L12: Entry 2 of 14

File: USPT

Feb 13, 2001

US-PAT-NO: 6189068

DOCUMENT-IDENTIFIER: US 6189068 B1

TITLE: Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Drawings
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☐ 3. Document ID: US 6079006 A

L12: Entry 3 of 14

File: USPT

Jun 20, 2000

US-PAT-NO: 6079006

DOCUMENT-IDENTIFIER: US 6079006 A

TITLE: Stride-based data address prediction structure

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 4. Document ID: US 5987561 A

L12: Entry 4 of 14

File: USPT

Nov 16, 1999

US-PAT-NO: 5987561

DOCUMENT-IDENTIFIER: US 5987561 A

TITLE: Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 5. Document ID: US 5978907 A

L12: Entry 5 of 14

File: USPT

Nov 2, 1999

US-PAT-NO: 5978907

DOCUMENT-IDENTIFIER: US 5978907 A

TITLE: Delayed update register for an array

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 6. Document ID: US 5968169 A

L12: Entry 6 of 14

File: USPT

Oct 19, 1999

US-PAT-NO: 5968169

DOCUMENT-IDENTIFIER: US 5968169 A

TITLE: Superscalar microprocessor stack structure for judging validity of predicted subroutine return addresses

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 7. Document ID: US 5881278 A

L12: Entry 7 of 14

File: USPT

Mar 9, 1999

US-PAT-NO: 5881278

DOCUMENT-IDENTIFIER: US 5881278 A

**** See image for Certificate of Correction ****

TITLE: Return address prediction system which adjusts the contents of return stack storage to enable continued prediction after a mispredicted branch

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 8. Document ID: US 5878255 A

L12: Entry 8 of 14

File: USPT

Mar 2, 1999

US-PAT-NO: 5878255

DOCUMENT-IDENTIFIER: US 5878255 A

TITLE: Update unit for providing a delayed update to a branch prediction array

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 9. Document ID: US 5875324 A

L12: Entry 9 of 14

File: USPT

Feb 23, 1999

US-PAT-NO: 5875324

DOCUMENT-IDENTIFIER: US 5875324 A

TITLE: Superscalar microprocessor which delays update of branch prediction information in response to branch misprediction until a subsequent idle clock

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 10. Document ID: US 5860104 A

L12: Entry 10 of 14

File: USPT

Jan 12, 1999

US-PAT-NO: 5860104

DOCUMENT-IDENTIFIER: US 5860104 A

TITLE: Data cache which speculatively updates a predicted data cache storage location with store data and subsequently corrects mispredicted updates

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 11. Document ID: US 5854921 A

L12: Entry 11 of 14

File: USPT

Dec 29, 1998

US-PAT-NO: 5854921

DOCUMENT-IDENTIFIER: US 5854921 A

TITLE: Stride-based data address prediction structure

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 12. Document ID: US 5822574 A

L12: Entry 12 of 14

File: USPT

Oct 13, 1998

US-PAT-NO: 5822574

DOCUMENT-IDENTIFIER: US 5822574 A

TITLE: Functional unit with a pointer for mispredicted resolution, and a
superscalar microprocessor employing the same

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 13. Document ID: US 5764946 A

L12: Entry 13 of 14

File: USPT

Jun 9, 1998

US-PAT-NO: 5764946

DOCUMENT-IDENTIFIER: US 5764946 A

TITLE: Superscalar microprocessor employing a way prediction unit to predict the
way of an instruction fetch address and to concurrently provide a branch prediction
address corresponding to the fetch address

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 14. Document ID: US 5752069 A

L12: Entry 14 of 14

File: USPT

May 12, 1998

US-PAT-NO: 5752069

DOCUMENT-IDENTIFIER: US 5752069 A

**** See image for Certificate of Correction ****

TITLE: Superscalar microprocessor employing away prediction structure

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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Term	Documents
(11 AND 6).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	14
(L11 AND L6).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	14

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